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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09 872,798	06/02/2001	Hirofumi Harada	S004-4310	4143

7590

05/30/2003

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EXAMINER

LE, THAO X

ART UNIT

PAPER NUMBER

2814

DATE MAILED: 05/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/872,798

Applicant(s)

HARADA, HIROFUMI

Examiner

Thao X Le

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2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 April 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 and 10-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 and 10-18 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☒ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

1. Claims 10-11 and 13-18 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6211549 to Funaki et al.

Regarding to claim 10, Funaki discloses a vertical MOS transistor in fig. 2 comprising: a semiconductor substrate 22 having a first conductivity type, an epitaxial layer 21 having the first conductivity type formed on the semiconductor substrate 22, a body region 24 having a second conductivity type formed on the epitaxial growth layer 21, a trench 28, column 6 line 20, extending through at least the body region 24 and extending into the epitaxial layer 21, a gate insulator film 29, column 6 line 28, formed in the trench and having a sidewall and a bottom surface defining a first U-shaped void; and a gate 30, column 6 line 31, formed of a first gate material disposed in the U-shaped void of the gate insulator so that the first gate material 30 has a second U-shaped void, and a second gate material 29a comprised of an insulating material,

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column 6 line 42, disposed in the second U-shaped void so as to be surrounded by the gate insulator 29 and first gate material 30, fig. 2.

Regarding to claims 11, 13-14, Funaki discloses a vertical MOS transistor in fig. 2 wherein the first gate material 30 comprises polycrystalline silicon, column 6 line 31, and the second gate material 29a comprises one of an oxide of silicon oxide, column 6 lines 33 and 42, wherein the gate insulator 29 is formed of silicon oxide, column 9 line 33, wherein the second material 29a is in contact with the first gate material 30.

Regarding to claims 15-18, Funaki discloses a vertical MOS transistor in fig. 2 further comprises a source region 25 having the first conductivity type formed in a upper surface of the body region 24 to surround the trench and in contact with the gate insulator 29, wherein a source electrode 37 connected the source region 25, and drain electrode 40 connected to the semiconductor substrate, wherein the trench 28 is formed in a U shape.

2. Claims 10-15, 18 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6461918 to Calafut.

Regarding to claim 10, Calafut discloses a vertical MOS transistor in fig. 5 comprising: a semiconductor substrate 320 having a first conductivity type, an epitaxial layer 325 having the first conductivity type formed on the semiconductor substrate 320, a body region 305 having a second conductivity type formed on the epitaxial growth layer 325, a trench 310, column 4 line 38, extending through at least the body region 305 and extending into the epitaxial layer 325, a gate insulator film 312, column 4 line 42, formed in the trench and having a sidewall and a bottom surface defining a first U-shaped void; and a gate 340/350/345, fig. 5, formed of a first gate material disposed in the U-shaped void of the gate insulator so that the first gate material

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has a second U-shaped void, and a second gate material 355 comprised of an insulating material, column 4 line 65 and column 5 line 4, disposed in the second U-shaped void so as to be surrounded by the gate insulator 312 and first gate material, fig. 5.

Regarding to claims 11-15, 18 Calafut discloses a vertical MOS transistor wherein the first gate 340/350/345 material comprises polycrystalline silicon, column 4 line 51, and the second gate material 355 comprises SiO_2 , wherein first and second gate material fill up the trench so that there is substantially no void at the top surface of the gate, fig. 5, wherein the gate insulator 312 is SiO_2 , column 4 line 42, wherein the second gate material 355 is in contact with the first gate material, fig. 5, wherein the vertical MOS further comprises a source region 330 having the first conductivity type formed in the upper surface of the body region 305 to surround the trench and in contact with the gate insulator 312, wherein the trench is formed in a U shape.

Allowable Subject Matter

3. Claim 1 are allowed because the prior art of record does not disclose all the limitations of the claim 1 including a gate insulating film formed along an upper surface of the body region and a second gate material of silicon oxide film filling a remaining portion of the internal void not filled by the polycrystalline silicon gate.

Conclusion

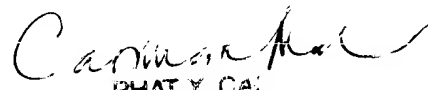
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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X Le whose telephone number is 703-306-0208. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M Fahmy can be reached on 703-308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Thao X. Le
May 21, 2003


PHAT X. CAI
PRIMARY EXAMINER